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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/855,240	05/15/2001	Louis L. Hsu	YOR920000660US1 (13959)	9000

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EXAMINER
MCLEAN-MAYO, KIMBERLY N

ART UNIT	PAPER NUMBER
2187	5

DATE MAILED: 05/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/855,240	HSU ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on March 4, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung (USPN: 6,415,353).

Regarding claim 1, Leung discloses a high speed DRAM comprising a DRAM memory (Figure 1, References 0-63); a cache memory (Figure 1, Reference 187); a read register coupled between the cache memory and the DRAM for transferring data from the cache memory to the DRAM memory (Figure 1, Reference 188; C 8, L 62-65); a write register coupled between the DRAM memory and the cache memory, for transferring data from the DRAM memory to the cache memory (Figure 1, Reference 189; C 8, L 65-67; C 9, L 1-2); a first data bus set coupled between the cache memory and both the read register and the write register (Figure 1 - first bi-directional bus is comprised of the signal means used to transfer data between the cache, Reference 187, and the read register, Reference 188, and the signal means used to transfer data between the cache and the write register, Reference 189); a second data bus set coupled between the read register and the DRAM memory (signal means coupling References 0-63 to Reference 188 in

Figure 1); a third data bus coupled between the DRAM memory and the write register (signal means coupling References 0-63 to Reference 189 in Figure 1). Leung does not explicitly disclose a first bi-directional data bus set coupled between the cache memory and both the read register and the write register. However, bi-directional data buses are well known in the art for reducing signal lines by allowing a single set of signals to be used for reading and writing, thereby providing efficiency. Hence, it would have been obvious to one of ordinary skill in the art to use a bi-directional bus in Leung's system for the desirable purpose of efficiency.

Regarding claim 2, Leung discloses a single port SRAM (C 8, L 8-62).

Regarding claim 4, Leung discloses a sixth data bus (signal means coupling Reference 188 to Reference 190 via References 191,192) coupling the read register to a data output from a circuit (Figure 1, Reference 190), and a seventh data bus (signal means coupling Reference 189 to Reference 190 via Reference 194) coupling a data input to the circuit to the write register.

Regarding claim 5, Leung discloses an eighth data bus, (signal means coupled to Reference 192 and 193, which effectively couples the write register to outside data busses DQ[31:0] when Reference 193 couples signal DB[255:0] to Reference 189), which couples the write register to outside data buses (Figure 1, DQ[31:0] coupled to Reference 190).

Regarding claims 6 and 10, Leung discloses a multiplexer switching between inputs received from the sixth data bus from the read register and the eighth data bus from the write register and

outputs data on a ninth data bus coupled to outside data busses (Figure 1, Reference 192, outputs data to outside DQ[31:0] via References 191,190).

Regarding claim 7 and 9, Leung discloses a read buffer coupling the read register to the DRAM memory through a tenth bus (Figure 1, Reference 172).

Regarding claim 8, Leung discloses an eleventh data bus coupling the DRAM memory to a write buffer which is coupled through the third data bus to the write register (Figure 1, Reference 171).

Regarding claim 11, Leung discloses data flow through the bi-directional bus in a first direction from the cache memory to the read register, and data flow through the bi-directional bus in a second opposite direction from the write register to the cache memory such that opposite direction data flows share the same bi-directional data bus in different cycles [clock cycles] (C 9, L 3-7 – the cache is a single port cache and thus data can only be either read or written in one clock cycle).

Regarding claim 12, Leung discloses data flow from the read register to the DRAM memory (C 10, L 25-44 - cache write-back) in a first cycle and data flow from the DRAM memory to the write register in a second cycle to share access to the DRAM memory in different cycles (C 10, L 45-50 - replace old cache data for a cache miss).

Regarding claims 13, 19 and 21, Leung discloses for a read miss operation, a new set of data is retrieved from the DRAM memory to replace the old data in the cache memory and also sent to outside data buses through an output read buffer (C 10, L 25-64) and during a first cycle of data flow (first cycle comprises time period for transferring data to Reference 192 from Reference 187 for a read), data flows from the cache memory through the first and fourth buses (fourth bus is signal line output from Reference 188 to DA[255:0]) and is latched into the read register (C 9, L 55-59) and data coming from the DRAM memory are latched into the write register through the third bus (C 10, L 45-49) and in a second cycle (second cycle comprises time period for transferring data from References (0-63) to Reference 189), the directional flows of the data are reversed through the first and fourth buses and also through the third bus.

Regarding claims 14, 20-21, Leung discloses for a write miss operation, a new set of data are written into the cache memory to replace retired data, partly from outside data buses via a write buffer and the rest of the data are from the DRAM memory and these data are merged in the write register (C 10, L 65-67; C 11, L 1-43).

Regarding claims 15 and 17, Leung discloses for a read hit operation, transferring data nondestructively from the cache memory through the read register to an output read buffer via a multiplexer and according to a column address, wherein only a portion of the data are transferred to outside data buses (C 9, L 55-67).

Regarding claims 16 and 18, Leung discloses for a write hit operation, a new set of data is transferred to the cache and overwrites a portion of the old data therein (C 10, L 1-24).

Regarding claim 3, Leung discloses the limitations cited above in claim 1, however, Leung does not disclose a multiplexer coupling the cache memory to either of the read register or the write register and a fourth data bus for coupling the multiplexer to the read register and a fifth data bus for coupling the multiplexer to the write register. However, it is known in the art to couple elements individually to a multiplexer via separate buses and to couple the elements to a device via the multiplexer. This structure provides a simple control mechanism for allowing two elements to share a signal line coupled to a device. Leung does not explicitly disclose control means for sharing the bi-directional bus. Hence, it would have been obvious to one of ordinary skill in the art to provide a multiplexer coupling the cache memory to either of the read register or the write register and a fourth data bus for coupling the multiplexer to the read register and a fifth data bus for coupling the multiplexer to the write register for the desirable purpose of providing a simple means for ensuring only one element has access to the shared bus.

Response to Arguments

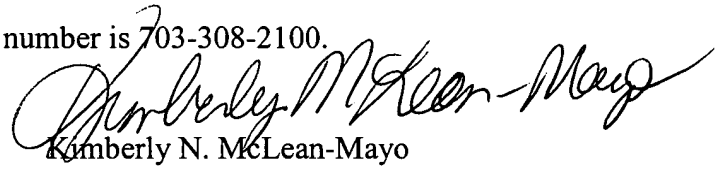
4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.



Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

May 12, 2003